IL0305911
IB/2004/050718

Europäisches Patentamt
European Patent Office
Office européen des brevets

Bescheinigung Certificate Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. Patent application No. Demande de brevet n°

03101537.3 ✓

PRIORITY DOCUMENT
SUBMITTED OR TRANSMITTED IN COMPLIANCE WITH RULE 17.1(a) OR (b)

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

Anmeldung Nr:
Application no.: 03101537.3
Demande no:

Anmeldetag:
Date of filing: 27.05.03
Date de dépôt:

Anmelder/Applicant(s)/Demandeur(s):

Koninklijke Philips Electronics N.V.
Groenewoudseweg 1
5621 BA Eindhoven
PAYS-BAS

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Operating long on-chip buses

In Anspruch genommene Priorität(en) / Priority(ies) claimed /Priorité(s) revendiquée(s)
Staat/Tag/Aktenzeichen/State/Date/File no./Pays/Date/Numéro de dépôt:

Internationale Patentklassifikation/International Patent Classification/
Classification internationale des brevets:

G06F13/00

Am Anmeldetag benannte Vertragstaaten/Contracting states designated at date of filing/Etats contractants désignées lors du dépôt:

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT RO SE SI SK TR LI

Operating long on-chip buses

The present invention relates to operating long on-chip buses.

Integrating large system on chip (SOC) devices can be a great challenge as the environment on the chip becomes more and more noisy. At the same time as the technology shrinks, on-chip wires are becoming narrower and denser, and their RC time constants are increasing. This leads to worsening delay over long interconnect runs. Such delays call for techniques which will enable on-chip buses to run at highest possible speed allowed by the environment.

Typically, inverters or buffers are used as receivers at the receiving end of a bus. Figure 1 of the accompanying drawings schematically illustrates a bus on an integrated circuit device, the bus including a series of bus lines 4 which are interconnecting wires between drivers 2 and receivers 6. Each bus line 4 connects a driver 2 to a corresponding receiver 6. Since the rise/fall times are typically excessively long (for example, see figure 2 of the accompanying drawings; "IN" refers to input to bus driver and "LINEOUT" refers to output at the end of a 10mm long bus on Metal 2 CMOS12) at the receiving end, the speed of sensing transitions on the bus is very slow, if the switching threshold of the inverter/buffer receiver is at Vdd/2 (half the supply voltage).

It is proposed to change this threshold (lower/raise) for both the rising and falling edge transitions so as to achieve fast sensing as well as achieve robust signaling in noisy environment. Changing the thresholds may cause the receiver to sense glitches caused by crosstalk, which are highly undesirable. In the case of very noisy environment the threshold can be raised above Vdd/2. Thus there exists a possibility to vary threshold of the receiver in order to achieve robust signaling at the highest possible speed in that environment.

Schmitt triggers are often used for rejecting noise wherein hysteresis of the transfer characteristics is utilized to raise the threshold for rising transitions and vice-versa

for falling transitions at its input. However, this only provides variation of threshold in one direction and cannot be calibrated. In the proposed scheme the threshold can be varied in both the directions (raise or lower from Vdd/2 point) to suit the conditions on the chip. Since the calibration is done on the chip it takes care of process variations on both the front-end processing as well as on the backend processing.

According to one aspect of the present invention, there is provided a bus system for an integrated circuit device, the bus comprising a plurality of bus lines (4) each of which connects a driver circuit (2) and a receiver circuit (6), characterized in that each receiver circuit comprises:

- a first detector (10) operably connected to receive a data signal from an associated bus line (4), and operable to detect a rising transition of the data signal with respect to a first threshold level, and to produce a first output signal upon detection of such a rising transition;
- a second detector (12) operably connected to receive the data signal, and operable to detect a falling transition of the data signal with respect to a second threshold level, and to produce a second output signal upon detection of such a transition; and
- output means operable to output the first or second output signal as a receiver output signal.

According to another aspect of the present invention, there is provided a method of operating a bus system for an integrated circuit device, the bus comprising a plurality of bus lines (4) each of which connects a driver circuit (2) and a receiver circuit (6), characterized in that the method comprises:

- receiving a data signal from a bus line (4);
- detecting a rising or falling transition of the data signal with respect to first and second threshold levels respectively;
- producing a first output signal upon detection of a rising transition, or producing a second output signal upon detection of a falling transition; and

outputting the first or second output signal as a receiver output signal.

Figure 1 illustrates schematically a bus on an integrated circuit device;

Figure 2 illustrates RC response at the receiving end of a 10mm wire on an M2,0.13µm CMOS circuit;

Figure 3 illustrates a receiver circuit;

Figure 4 illustrates the receiver circuit of Figure 3 in more detail;

Figure 5 illustrates a scheme with a dummy bus;

Figure 6 illustrates a scheme which uses the same bus for calibration;

Figure 7 illustrates a state diagram for the calibration circuit;

Figure 8 illustrates glitch detection by using convention latches;

Figure 9 illustrates some of the simulation waveforms.

Figure 3 illustrates a receiver circuit for use in embodiments of the present invention. The receiver of Figure 3 has first and second detectors 10 and 12. The first detector 10 is sensitive to transitions occurring from low to high and the second detector from high to low. Both detectors are connected to receive the data signal transmitted on the bus wire 4, and are operable to detect respective transitions of that signal on the bus wire 4. The detectors have respective outputs which are combined via a multiplexer 14. The multiplexer 14 has a select line controlled by the previous data on the bus wire 4. The previous data value is stored in a state element 16. A state element could be a flip-flop, latch or a delay line.

The thresholds of the first and second detectors of the receiver are controlled by a control word, which is generated by a calibrator (not shown in Figure 3).

The receiver circuit is shown in more detail in Figure 4. It consists of two inverters whose thresholds can be controlled independently by the calibrator. The calibrator applies the control word, which selects the number of transistors T10, T12 to be used in parallel in a respective pull down/up networks in the inverters of the receiver. This tunes the threshold of the inverters for rising and falling transitions respectively. The selection of signal to be output from the multiplexer is based on the previous value of the output, which is stored in the state element 16. For example, if the present value is high then the multiplexer 14 selects the output of the detector (inverter) 12 which is sensitive to falling transitions.

The calibrator 18 uses either a dummy bus as shown in Figure 5, or the main bus with slight modifications in the driver circuit (which then uses a multiplexer) as shown in Figure 6, to simulate worst case switching conditions on the chip. The simulation enables the calibrator to set the control word to an appropriate value. The calibration can be done once during power-up or during chip initialization. The dummy bus 20 technique shown in Figure 5 involves the use of an extra set of bus drivers 22, bus lines 24, and bus receivers 26 to simulate the cross talk to be executed on the real bus 2,4,6.

The calibrator circuit is preferably implemented as a finite state machine (shown in Figure 7), which applies signals on primary bus wires (aggressor wires) and measures the crosstalk on at least one secondary bus wire (victim wire). If a glitch is detected which can possibly cause failure then it changes the threshold of the receiver 10, 12 and re-applies the signals to the primary bus wires. This procedure is repeated until the output of the receiver circuit.

A glitch sensor circuit 28, which includes a pair of latches, is used to capture the glitches. See Figure 8. The first latch 30, is transparent low and is connected to 'b' in Figure 4. The other latch 32 is transparent high and is connected to 'a' in Figure 4. Output from one of the latch is selected by a multiplexer 34 based on the logic level on the victim wire M which is generated by the calibrator 18.

Figure 7 illustrates the state diagram of the calibrator, 'M' and 'S' represent the signals on victim and aggressor wires respectively. Calibration starts when 'Ca' is asserted. 'T' is the reset signal to the glitch capturing latches. 'C' is a signal which goes high whenever the latches detect appreciable glitch at their inputs. 'CW1' and 'CW2' are the signals which are used to increment a counter in the calibrator 18 that generates the control word for the receiver circuit threshold adaptation.

As the calibration proceeds it can be seen with reference to Figure 9 that the thresholds of the receiving inverters are adjusted so that the amplitude of glitches decrease.

The simulations are performed on a 10mm long bus at minimum spacing and minimum width on Metal 2 in CMOS12 TSMC technology. In a typical process case, 10% performance gain can be achieved for the bus structure specified above. On the other hand in a very noisy environment which may occur due to process variations the threshold may be raised by the calibrator and hence avoid glitches at the output of receiver. In this case penalty will have to be paid in terms of increase in worst case delay along the bus. Glitch prevention may be very essential at the output of the receiver, especially in asynchronous circuits.

CLAIMS:

1. A bus system for an integrated circuit device, the bus comprising a plurality of bus lines (4) each of which connects a driver circuit (2) and a receiver circuit (6), characterized in that each receiver circuit comprises:

- a first detector (10) operably connected to receive a data signal from an associated bus line (4), and operable to detect a rising transition of the data signal with respect to a first threshold level, and to produce a first output signal upon detection of such a rising transition;
- a second detector (12) operably connected to receive the data signal, and operable to detect a falling transition of the data signal with respect to a second threshold level, and to produce a second output signal upon detection of such a transition; and
- output means operable to output the first or second output signal as a receiver output signal.

2. A bus system as claimed in claim 1, wherein the output means comprises a multiplexer (14) operably connected to receive the first and second output signals, and operable to output the receiver output signal in dependence upon a previous receiver output signal.

3. A bus system as claimed in claim 1 or 2, wherein the first and second threshold levels are variable.

4. A bus system as claimed in claim 3, further comprising a calibrator (18) for adjusting the first and second threshold levels.

5. A bus system as claimed in claim 4, wherein the first and second detectors (10,12) include respective pluralities of transistors, and the calibrator (18) is operable to activate varying numbers of those transistors, in order to adjust the threshold levels.

6. A bus system as claimed in claim 4 or 5, further comprising a glitch sensor circuit 28) which is operable to detect glitches on at least one of the bus lines (4).

7. A bus system as claimed in claim 6, wherein the glitch sensor circuit (28) comprises a pair of latches (30,32) each having an output, and a multiplexer (34) operable to select one of the latch outputs for supply to the calibrator (18).

8. A bus system as claimed in claim 6 or 7, wherein the calibrator (18) is operable to supply test signals to the bus lines, and the glitch sensor circuit (28) is operable to detect glitches on at least one bus line (4) and to supply a glitch signal to the calibrator (18), the calibrator (18) then being operable to adjust the threshold values of the detectors in dependence upon the glitch signal.

9. A bus system as claimed in claim 6 or 7, further comprising a test bus including a plurality of test drivers (22), and corresponding pluralities of bus lines (24) and receivers (26), the calibrator (18) being operable to supply test signals to the test bus lines (24), and the glitch sensor circuit (28) being operable to detect glitches on the test bus lines (24) and to supply a glitch signal to the calibrator (18), the calibrator then being operable to adjust threshold values of the detectors in dependence upon the glitch signal.

10. A method of operating a bus system for an integrated circuit device, the bus comprising a plurality of bus lines (4) each of which connects a driver circuit (2) and a receiver circuit (6), characterized in that the method comprises:

- receiving a data signal from a bus line (4);
- detecting a rising or falling transition of the data signal with respect to first and second threshold levels respectively;
- producing a first output signal upon detection of a rising transition, or producing a second output signal upon detection of a falling transition; and
- outputting the first or second output signal as a receiver output signal.

11. A method as claimed in claim 10, wherein the first or second output signal is output a multiplexer (14) operably connected to receive the first and second output signals, and operable to output the receiver output signal in dependence upon a previous receiver output signal.

12. A method as claimed in claim 10 or 11, wherein the first and second threshold levels are variable.

13. A method as claimed in claim 12, further comprising adjusting the first and second threshold levels.

14. A method as claimed in claim 13, wherein the first and second detectors (10,12) include respective pluralities of transistors, and the threshold levels are adjusted by activating varying numbers of those transistors.

15. A method as claimed in claim 13 or 14, further comprising detecting glitches on at least one of the bus lines (4).

16. A method as claimed in claim 15, wherein glitches are sensed using glitch sensor circuit (28) which comprises a pair of latches (30,32) each having an output, and a multiplexer (34) operable to select one of the latch.

17. A method as claimed in claim 15 or 16, further comprising supplying test signals to the bus lines, detecting glitches on at least one bus line (4), and adjusting the threshold values in dependence upon detected glitches.

18. A method as claimed in claim 15 or 16, further comprising supplying test signals to test bus lines (24), detecting glitches on the test bus lines (24), and adjusting the threshold values in dependence upon detected glitches.

ABSTRACT:

As technology scales, on-chip interconnects are becoming narrower, and the height of such interconnects is not scaling linearly with the width. This leads to an increase of coupling capacitance with neighboring wires, leading to higher crosstalk. It also leads to poor performance due to poor RC response at the receiving of the wire, which may even result in failure in very noisy environments. An adaptive threshold scheme is proposed in which receiver switching thresholds are adjusted according to the detected noise in bus lines. These noise levels are dependent on both the front-end processing (transistor performance) as well as on the backend processing (metal resistance, capacitance, width and spacing). The circuit therefore automatically compensates for process variations.

Fig. 3

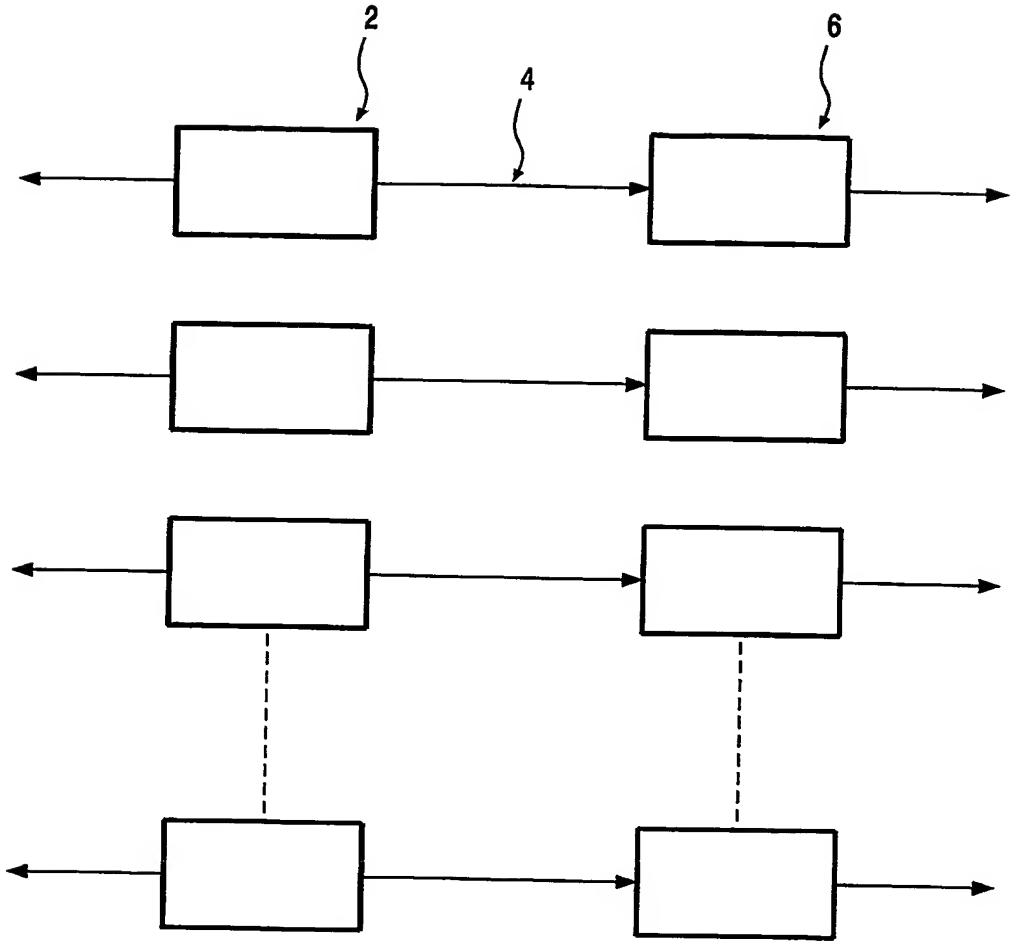

FIG. 1

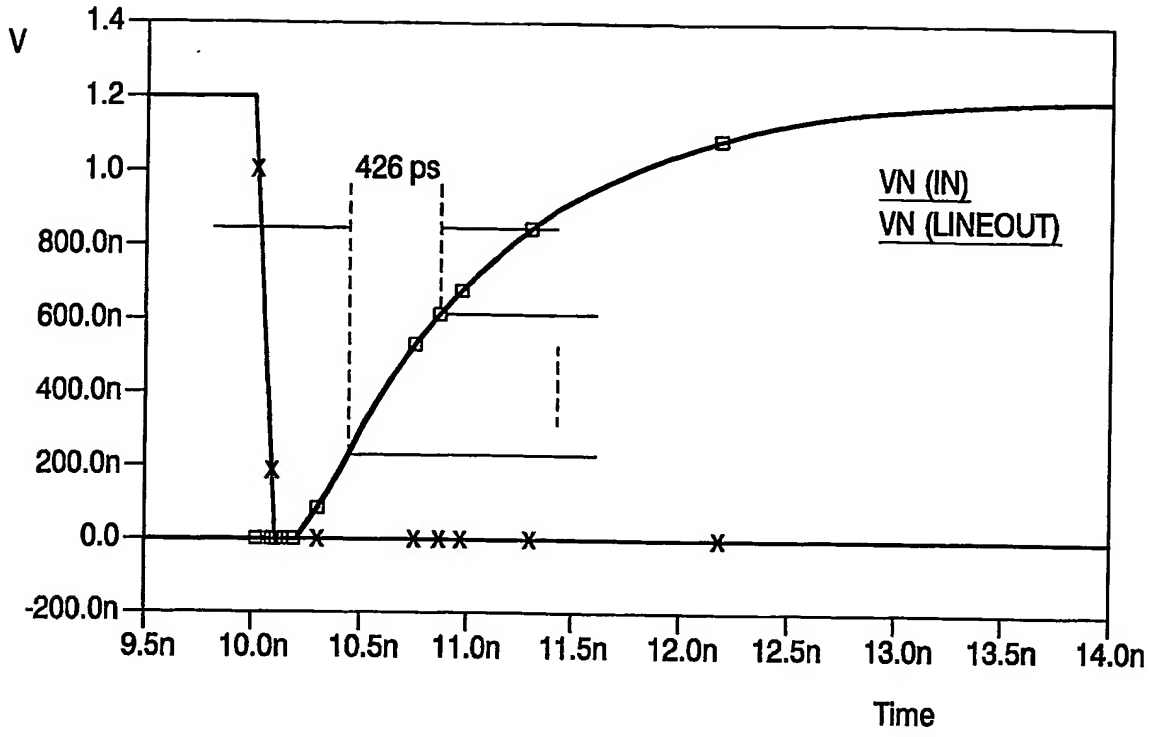
V
1.4
1.2
1.0
800.0n
600.0n
400.0n
200.0n
0.0
-200.0n
426 ps
VN (IN)
VN (LINEOUT)
9.5n
10.0n
10.5n
11.0n
11.5n
12.0n
12.5n
13.0n
13.5n
14.0n
Time

FIG. 2

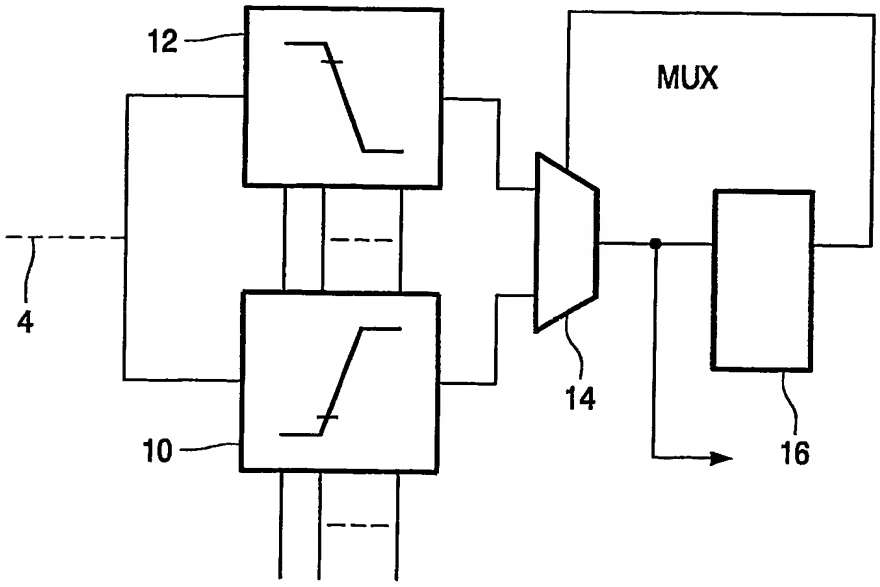
12
MUX
4
14
10
16

FIG. 3

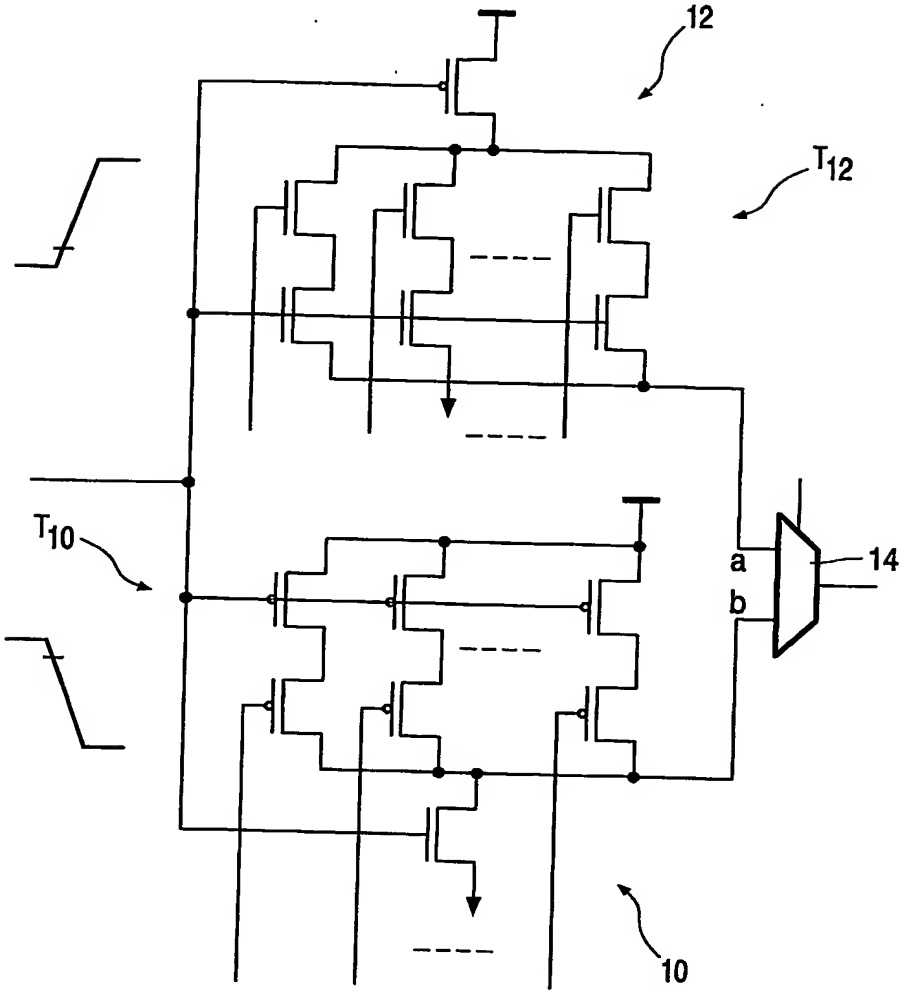

FIG. 4

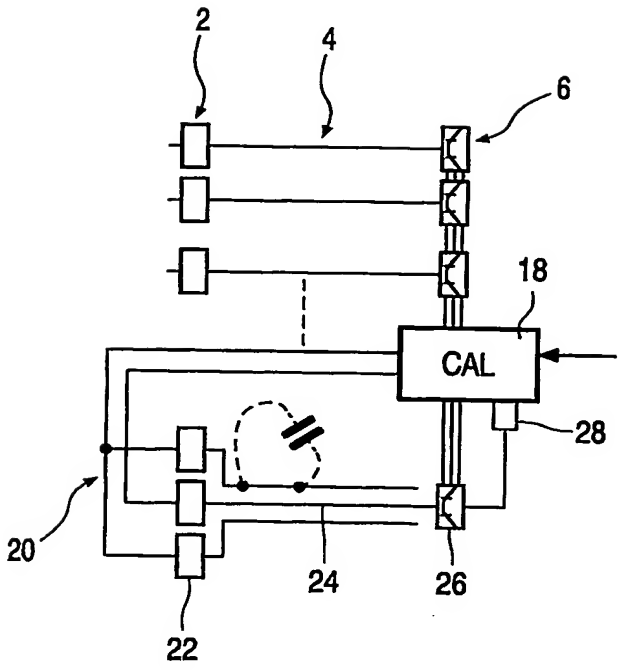

FIG. 5

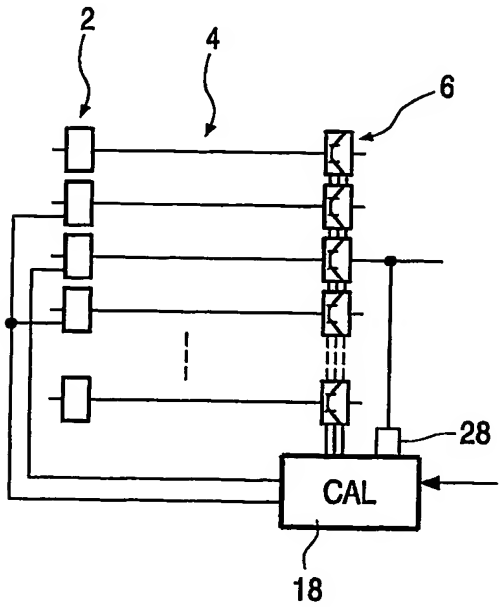

FIG. 6

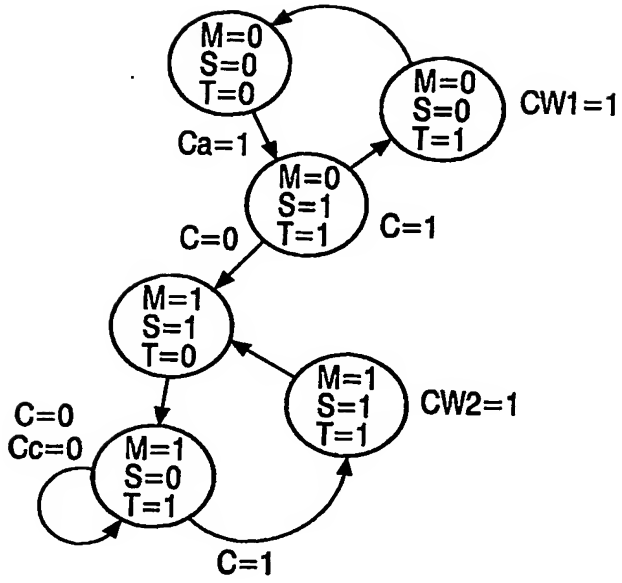
M=0
S=0
T=0
M=0
S=0
T=1
CW1=1
Ca=1
M=0
S=1
T=1
C=1
C=0
M=1
S=1
T=0
M=1
S=1
T=1
CW2=1
C=0
Cc=0
M=1
S=0
T=1
C=1

FIG. 7

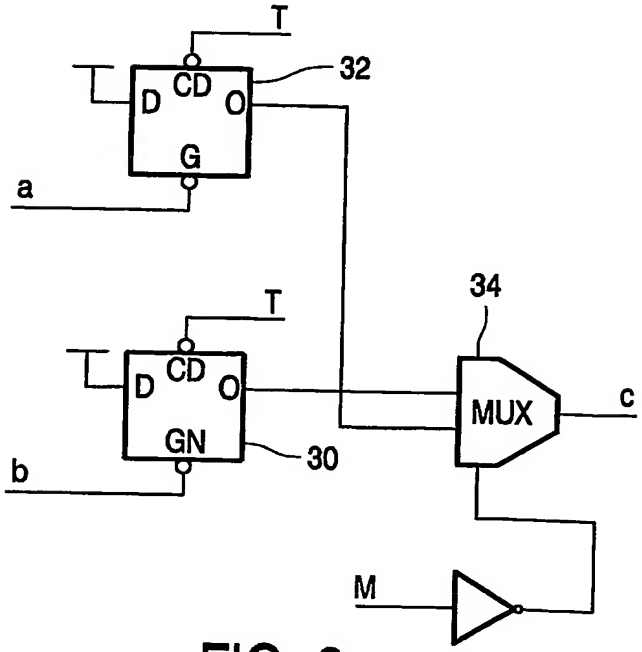
T
CD
D
O
G
32
a
T
34
CD
D
O
GN
MUX
c
30
b
M

FIG. 8

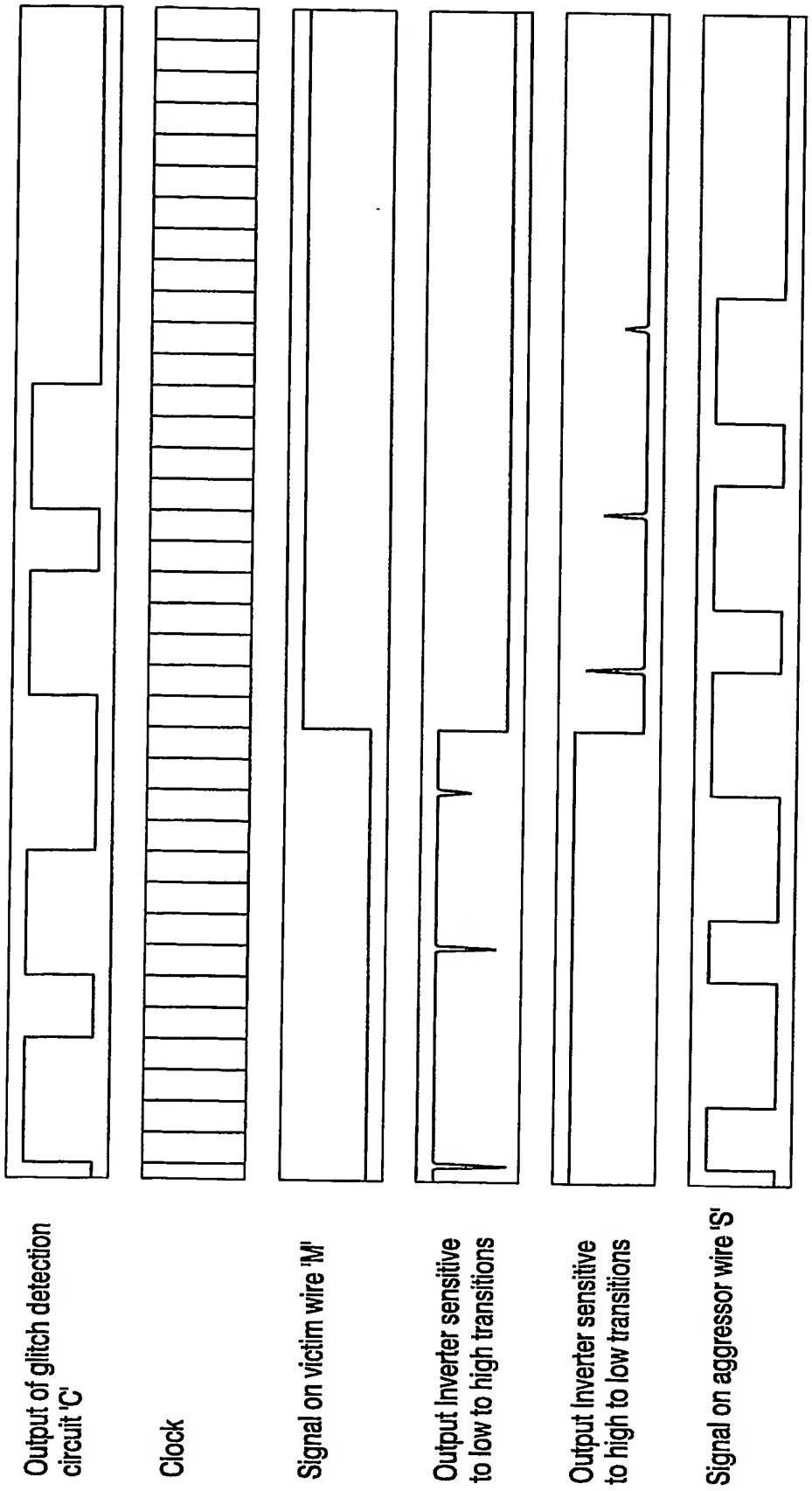
Output of glitch detection circuit 'C'
Clock
Signal on victim wire 'M'
Output Inverter sensitive to low to high transitions
Output Inverter sensitive to high to low transitions
Signal on aggressor wire 'S'

FIG. 9